METHOD FOR FORMING QUADRUPLE DENSITY SIDEWALL IMAGE TRANSFER (SIT) STRUCTURES

Field of the Invention

The present invention relates generally to the field of semiconductor manufacturing and, more specifically, to a method for forming a quadruple density sidewall image transfer (SIT) structure.

Description of the Related Art

Improvements in photolithography are driving continued shrinkage of dimensions in advanced semiconductor manufacturing. Photolithography is, however, finding progress increasingly expensive and difficult. Cost of advanced photo tooling continues to significantly increase and costs of consumables, such as resist, are also skyrocketing.

Meeting line width objectives has also required introduction of many new ways of enhancing traditional processes such as mask making and data preparation. These techniques introduce errors and, of course, additional expense.

It is highly desirable to provide a method which can meet or exceed line width control objectives for future technologies without requiring the use of new and more expensive tooling.

Summary of the Invention

A principal object of the present invention is to provide a method for forming a quadruple density sidewall image transfer (SIT) structure. Other important objects of the present invention are to provide such method for forming a quadruple density sidewall image transfer (SIT) structure substantially without negative effect and that overcome many of the disadvantages of prior art arrangements.

In brief, a method is provided for forming a quadruple density sidewall image transfer (SIT) structure. Oxide spacers are formed on opposite sidewalls of a first mandrel. The oxide spacers form a second mandrel. Then sidewall spacers are formed on opposite sidewalls of the oxide spacers forming the second mandrel. A pattern of the sidewall spacers is used to form the quadruple density sidewall image transfer (SIT) structure.

In accordance with features of the invention, the method of the invention enables formation of four well-controlled lines for each lithographically minimum pitch dimension. The method of the invention employs spacers-on-spacers, with one spacer formed utilizing oxidation to better balance line space sizes.

Brief Description of the Drawings

The present invention together with the above and other objects and advantages may best be understood from the following detailed description of the preferred embodiments of the invention illustrated in the drawings, wherein:

FIG. 1 is a side view of an exemplary starting structure for forming a quadruple density sidewall image transfer (SIT) structure in accordance with a method of the preferred embodiment; and

FIGS. 2A, 2B, and 3-9 are side views not to scale illustrating exemplary steps of a method for forming a quadruple density sidewall image

transfer (SIT) structure starting with the exemplary starting structure of FIG. 1 in accordance with the preferred embodiment.

Detailed Description of the Preferred Embodiments

Sidewall Image Transfer (SIT) techniques form conductors with very narrow widths or semiconductor devices with very short gate lengths without using critical photolithography. Sidewall Image Transfer has been proposed as a way to produce well-controlled images having sub-lithographic dimensions.

Use of sidewall spacers to define feature dimensions offers an opportunity to build two shapes using each starting shape since each starting shape, for example, printed using standard lithography, has two edges. Resulting features thus can have half the pitch possible using the same lithographic tools in a conventional printing process. It is desirable to extend the frequency doubling opportunity to even smaller dimensions.

In accordance with features of the preferred embodiment, an extension of the sidewall image transfer (SIT) approach is provided to enable formation of four well-controlled lines for each lithographically minimum pitch dimension. The method of the preferred embodiment is to employ spacers-on-spacers, with one spacer formed utilizing oxidation to better balance line space sizes.

Referring now to the drawings, in FIG. 1 there is shown an exemplary starting structure generally designated by the reference character 100 for forming a quadruple density sidewall image transfer (SIT) structure in accordance with the preferred embodiment. The exemplary starting structure 100 includes a substrate 102, such as a silicon substrate 102, a gate dielectric layer 104 and a gate conductor 106, such as polysilicon or gate conductor poly 106. Formed over the gate conductor poly layer 106 of the exemplary starting structure 100 includes an oxide hardmask layer 108, a poly etch stop layer 110, a first nitride layer 112, and a poly mandrel layer 114, such as polysilicon mandrel layer 114 capped with a second, thinner nitride layer 116. It should be understood that other materials than

polysilicon that are partially consumed in formation of the edge material could be used for the poly mandrel layer 114.

FIGS. 2A and 2B illustrates a print mandrel mask step generally designated by the reference character 200 with a respective pair of photoresist features 202, 204; and 202A, 204A formed on top of the exemplary starting structure 100 in accordance with the preferred embodiment. In FIG. 2A, the photoresist feature 202 has a width indicated by an arrow labeled F and is spaced apart from the photoresist feature 204 by a distance indicated by an arrow labeled F, for example, representing a lithographically minimum pitch dimension. In FIG. 2B, the photoresist features 202A, 204A are illustrated corresponding to a next processing step of FIG. 3.

FIG. 3 illustrates a next step of the method generally designated by the reference character 300 where the nitride layer 116 and the poly mandrel features 114 are etched corresponding to the photoresist features 202A, 204A and the photoresist features 202A, 204A are stripped.

Referring now to FIG. 4, in a next step of the method generally designated by the reference character 400 an oxide 402 is grown on each sidewall of the etched first mandrels 114. These oxides 402 defining oxide spacers form a second mandrel 402. The nitride films 112, 116 protect the second poly etch stop layer 110 and the top of the first mandrel 114 from oxidation.

FIG. 5 illustrates a next optional step of the method generally designated by the reference character 500. The grown oxide spacer mandrel 402 may not have an ideal profile where it meets the underlying nitride layer 112, and the grown oxide spacer mandrel 402 may not adhere properly to the underlying nitride 112. To alleviate this difficulty, while the grown oxide spacer mandrel 402 is still attached to the first poly mandrel 114, a thin oxide generally designated by the reference character 502, such as a thin Chemical Vapor Deposition (CVD) oxide 502 optionally is deposited and etched, if required, to fill any possible undercut profile of the thermally grown oxide spacer second mandrel 402.

Referring now to FIG. 6, in a next step of the method generally designated by the reference character 600, directional etching, such as RIE, is performed to remove the nitride film 116. The directional etching is stopped before breaking through the nitride film 112 and then the poly first mandrel 114 is removed. Poly removal can be done either all wet or dry poly removal with an isotropic component to guarantee full removal of the polysilicon mandrel 114.

FIG. 7 illustrates a sidewall spacer forming step 700 employing spacers-on-spacers in accordance with the preferred embodiment. A plurality of sidewall spacers 702 are formed using any suitable technique, such as by conformal deposition and directional etch of a nitride layer. Each sidewall spacer 702 is relatively thin. The sidewall spacers 702 are formed on sidewalls of each thermally grown oxide spacer second mandrel 402.

Referring now to FIG. 8, in a next step of the method generally designated by the reference character 800, the thermally grown oxide spacer second mandrel 402 is removed. The remainder of the nitride oxidation/etch-stop layers 112, 110, 108 then is removed by Reactive Ion Etching (RIE), while maintaining the profile and width of the nitride spacers 702.

Referring now to FIG. 9, in a final step of the method generally designated by the reference character 900, a pattern 902 of the nitride spacers 702 is transferred into the poly etch stop layer 110 and the oxide hardmask layer 108, and the nitride layer 112 is stripped. Produced now is the desired quadruple density (oxide) hardmask for gate conductor etch.

As is obvious to a person skilled in the art, the described method forms loops of only one dimension. Conventional SIT processing includes two additional masks of which the first mask trims the loops and the second mask adds larger shapes of any desired dimension. It should be understood that these conventional two additional masks apply to the method of the preferred embodiment also.

While the present invention has been described with reference to the details of the embodiments of the invention shown in the drawing, these details are not intended to limit the scope of the invention as claimed in the appended claims.